

An Evaluation of Chip Scale Packages for Missile Applications

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Executive Summary

The use of Chip Scale Packages (CSPs) and related package styles, such as direct chip attach (e.g., flip-chip) and ball grid arrays, will become extensive in consumer applications that require small volumes and low weight for electronics. These advanced electronics packaging approaches provide many advantages for missile and related applications that require minimal weight/volume and high electrical performance. The basic system engineering considerations of cost, performance (including reliability), and the like should determine the use of CSPs, and other advanced packages, since the conventional SMT will have continued availability for many years. To take advantage of these potential enhancements where necessary requires assessment of the reliability of circuit card assemblies that use CSPs to assure that they can meet system requirements. The primary areas that require additional testing and development include the printed wiring boards with high-density interconnections to support the CSP density, the flux impacts and cleaning processes, the IC chip reliability in a CSP assembly, and the CSP solder joint reliability for various constructions (particularly, large chip and array sizes). These issues will receive attention for commercial applications, but impacts on military applications will require some further efforts to address long term storage and high reliability. The potential improvements for long-term reliability afforded by conformal coatings will likely receive little evaluation outside

Reliability Assessments Required for CSPs

- High-density interconnection substrates (PWBs)
 - Microvias, decreasing line space/widths
- Cleaning processes for flux residues
 - No-clean flux impacts
- IC chip in CSP assembly
 - Sequential environments
- Solder joints for particular applications
 - General data may not apply
- Efficacy of conformal coatings in extending life

of military applications. Appendix B provides a plan to investigate these concerns, and provide data to support the insertion of CSPs into missile applications.

Background

To support the continuing increase in electronic processing power made possible by advances in integrated circuit (IC) device technology requires concomitant advances in the packaging technologies that interconnect the ICs. These interconnects include the connection from the IC to the first level package (e.g., quad flat pack, ball grid array, etc.), and the connection from the first level package to the second level package (e.g., printed wiring board). Present mainstream packages utilize wire bonds for the first level connection from the die. Various shapes of surface mount leads provide the second level connection to the printed wiring board substrate. Figure 1 illustrates the basic interconnects used in most packages today. Most die designs incorporate bond pads around the periphery of the die to support this packaging approach. The wire bond tool size limits the peripheral bond pad pitch to about 60 μm . This pitch could still provide 600 connections for a 10 mm chip, but at the second level interconnect the lead pitch cannot decrease below about 0.4 mm (Reference 7) due to assembly handling issues and printed wiring board limitations for pad spacing. Limiting the leads to 0.4 mm would require 240 mm of periphery, which would require a large space overhead penalty at 36 times the area of the 10 mm chip. An array pattern of interconnects to the printed wiring board at 0.4 mm pitch could provide the 600 connections in 24 mm² (about the size of a 5 mm chip). This space saving provides the impetus for development of area array packaging technologies.

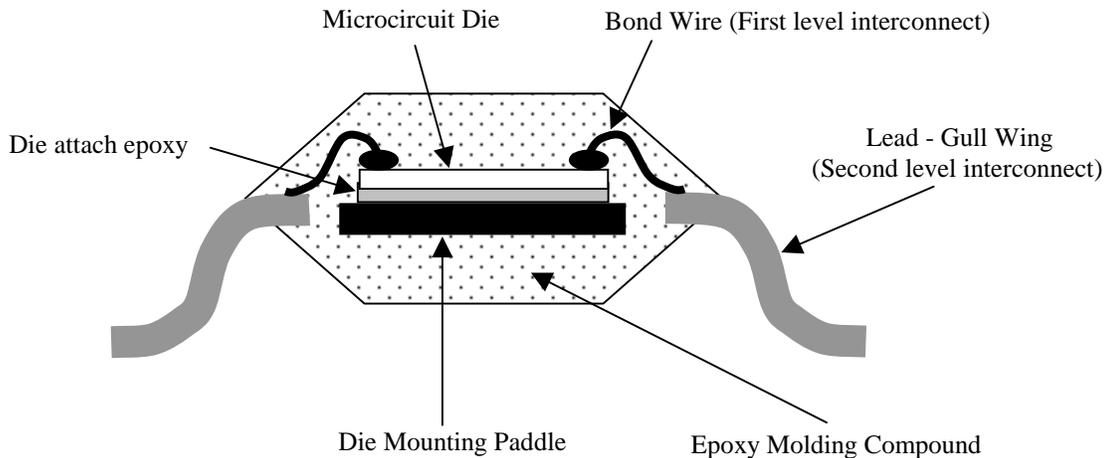


Figure 1. Conventional Surface Mount Packaging

A new class of first level package, referred to as Chip Scale Package (CSP), provides a method to meet the demands of increased connections on ICs and the goals of decreased size and weight of electronic assemblies. The generally accepted definition for CSPs is that they should not exceed 120% of the area or periphery of the

microcircuit chip itself. Designing a package to meet such constraints for large numbers of device connections generally requires the use of array interconnects from the IC package to the substrate (i.e., printed wiring board), as discussed above. For this reason most CSPs utilize array interconnection, but some devices with low interconnection count can be supported by peripheral connections and still meet the CSP size definition. Figure 2 illustrates a typical CSP design in production today. The total thickness of such a package is about 1 mm and extends beyond the edge of the chip by about 1 mm on each side.

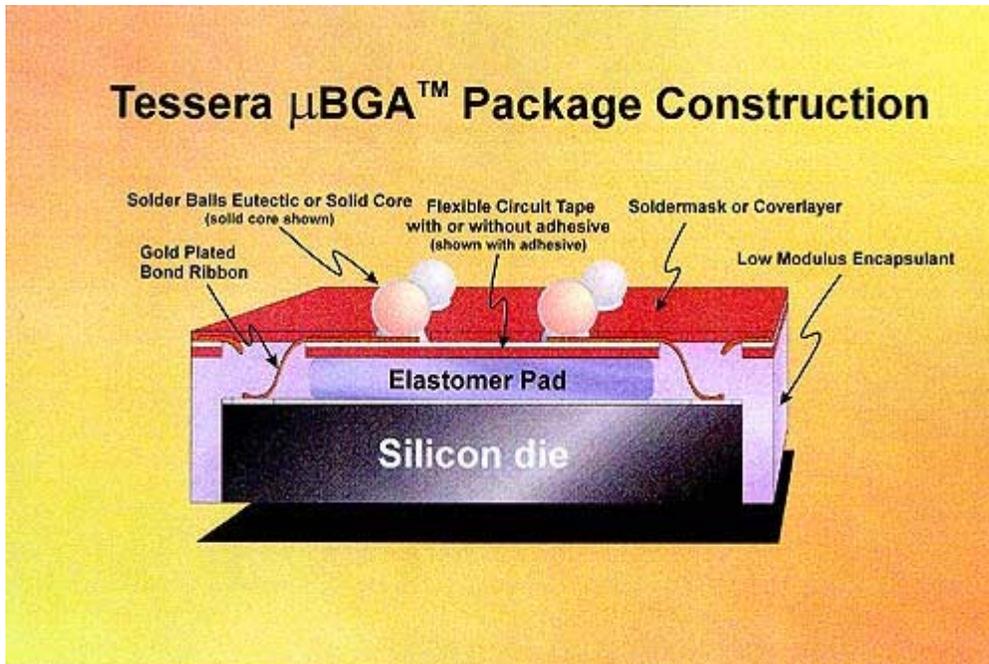


Figure 2. Example of CSP (Tessaera μBGA™) that utilizes an interposer; in this case a flex tape and elastomer pad.

With this smaller package area, CSPs will provide board space savings of about 75% compared to quad flat packs (QFPs), plastic leaded chip carriers (PLCCs), and small-outline ICs (SOICs), and by 50% compared to ball grid arrays (BGAs) and thin small-outline packages (TSOPs). Handheld telephony, camcorders, palmtop computers, memory cards, and similar applications represent the primary market drivers at this time for CSPs (Reference 2). One forecast indicates increased CSP usage from 419 million units in 1998 to 3.5 billion units in 2001 (Reference 3). The combination of CSP, BGA, and DCA will reach 20% of all parts used in 2002, according to Electronic Trend Publications, Inc., or a total of about 18 billion parts. Conventional surface mount packages, including QFPs and SOICs, will represent about 70% of the part usage at about 65 billion parts. Figure 3 shows one company's assessment for the need and adoption of CSPs. The Semiconductor Industry Association (SIA) 1997 Technology Roadmap projects the need for research in 0.3 mm pitch arrays now to support

incorporation into products in 2003 that require over 400 interconnects between the IC and the substrate.

Area Array Package's Roadmap

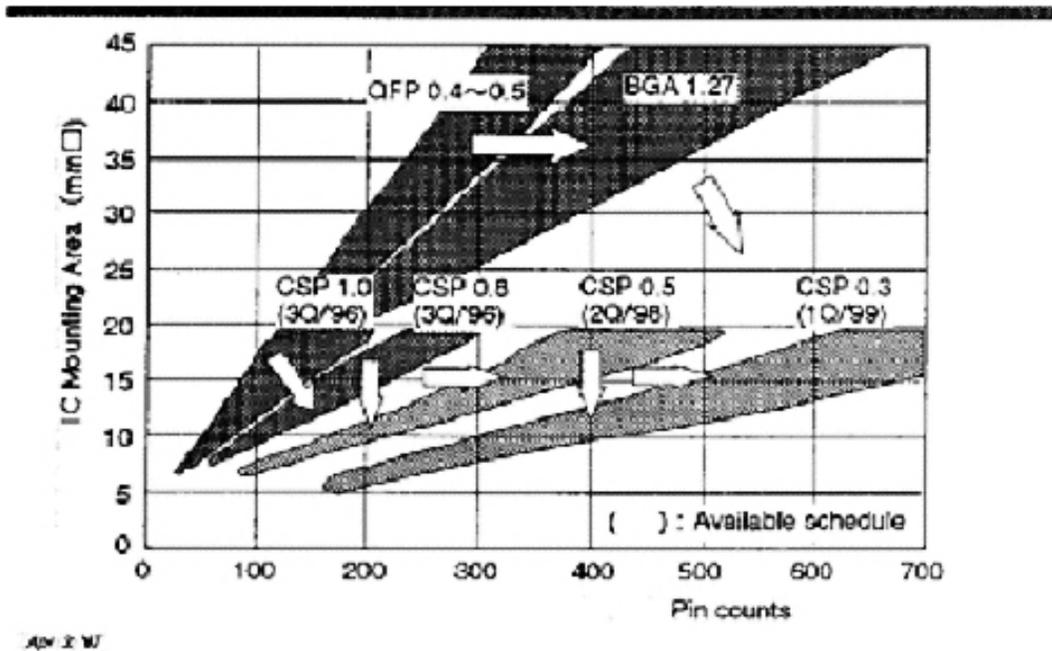


Figure 3. Representative roadmap for progression of integrated circuit packaging.

The significant reductions in board space and weight provided by CSPs offer attractive options for military systems, particularly for missiles, since missile applications often have severe weight and space constraints for electronics. In addition, CSPs offer clear electrical performance, packaging volume, and weight advantages. For instance, Sharp reports inductance reduction from 5.6 nH for a TSOP to 4.0 nH for their CSP that uses wire bonds and a polyimide interposer (Reference 7). Likewise, Sharp's package demonstrated thermal resistance (junction to ambient) of 54°C/W compared to 123°C/W for a TSOP with similar number of connections. To leverage the commercial use of these new packaging technologies in missile systems requires an assessment of the reliability of CSPs in military applications. To understand what efforts should be pursued to evaluate CSPs, this paper will investigate the various CSP constructions, and the impact on the next level interconnects and packages (i.e., board level).

Advantages of CSP
Over Conventional Surface Mount Packages

- Lower parasitic signal degradation from chip to substrate
- Package area nearly the size of the chip
 - Typical substrate area reduction of 75%
- Better thermal path to the substrate
- Easier handling for high interconnect counts/densities

CSP Types and Next-Level Assembly

Many different varieties of CSPs exist to varying degrees of use. They employ wire bonds, tape automated bonding, and bump interconnects at the die level. They may utilize flexible and rigid interposers to redistribute signals (from periphery into an area array) and provide thermomechanical isolation, or merely use a redistribution layer that provides essentially no thermomechanical isolation (relying on the solder ball to provide isolation). Some designs include the use of a conventional lead frame and wire bond first level interconnects (but likely limited in I/O count advancement). Figures 2, 4, and 5 illustrate the construction implemented on a variety of CSPs. Joint Industry Standard J-STD-012 (Reference 8) provides a description of the main varieties of CSPs and some discussion on assembly and reliability considerations. CSPs as a class use many diverse materials, constructions, and manufacturing processes, so that specific assessments regarding reliability, and other performance parameters, require evaluation of particular packages.

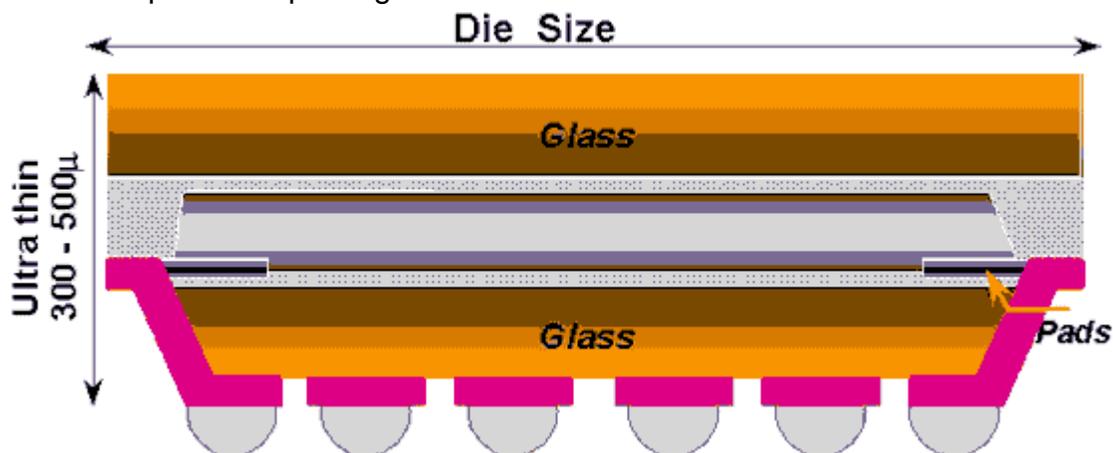


Figure 4. Example of wafer level CSP (ShellCase)

The CSP designs share common properties of minimal protection for the die from the package ambient conditions, and a complex combination of materials with varying thermal expansion coefficients (see Table 1). With the minimal protection of the chip afforded by the CSP, the IC chip passivation becomes a more critical link in the device reliability. For instance, the UltraCSP™ package from FlipChip Technologies adds only two thin films of polyimide over the chip to serve as the dielectric for redistributing the chip peripheral bond pads to an area array interconnect. Moisture diffuses through polyimide at room temperature with a diffusion coefficient of $5 \times 10^{-9} \text{ cm}^2/\text{s}$, and the activation energy for diffusion is 0.25 eV (Reference 9). This transport rate provides the opportunity for moisture to react with the IC chip surfaces, particularly over long storage times. In addition, such a design provides very little strain relief for the thermal expansion mismatch between the Silicon IC chip and a typical FR-4 epoxy-glass substrate, so that large I/O counts on large die may not provide reliable solder joints under extensive thermal cycling. Because the I/O pitches become small and the I/O density increases for CSPs, the substrate capability to meet such demands requires assessment, as well as the assembly capabilities of manufacturers.

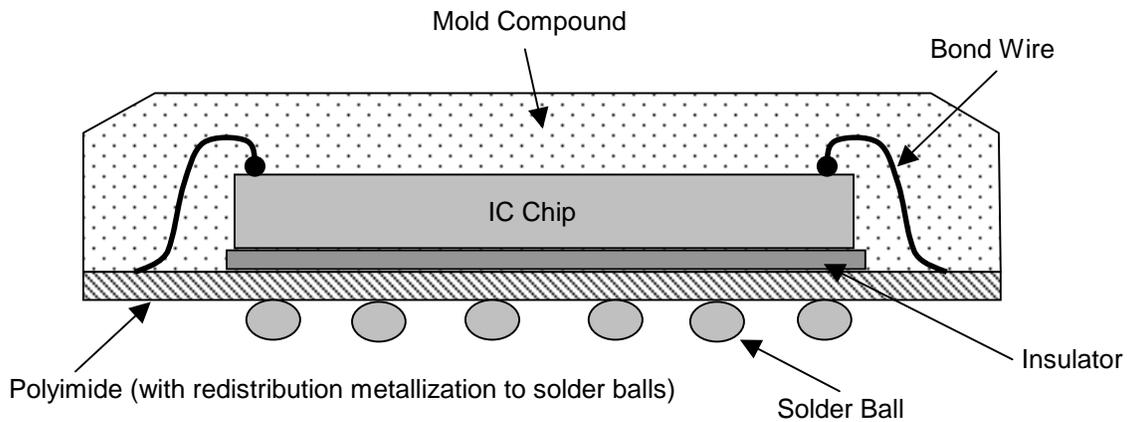


Figure 5. Cross-section of CSP utilizing traditional wire bonding (with special wire shape control).

The present advanced Surface Mount Technology assembly infrastructure can support CSPs, since 0.5 mm and 0.4 mm pitch peripheral lead devices have been introduced (Reference 5), and CSPs generally incorporate pitches greater than 0.38 mm. Present solder pastes and paste application approaches have demonstrated solder joint quality levels in the 10 ppm defect range (Reference 5), which supports high solder joint yield for over 1000 joints on an assembly. For the mainstream CSPs envisioned for the next 10 years, the assembly capabilities existing now should suffice. While part placement and solder application capabilities exist for CSP, the efficacy of cleaning processes for removing flux residues in the small space between the substrate and the bottom of the package, and the impact of no-clean fluxes on CSPs require further evaluation and perhaps further process development.

The present PWB technology design rules and capability can support pitches down to about 0.65 mm (reference 5), but some test data (reference 6) has shown that PWB vias in the range of 15 mils (0.38 mm) fail in temperature cycling before the solder connects in BGAs. The PWB vias could represent the weakest link for high-density interconnection assemblies. The SIA Technology Roadmap (Reference 4) anticipates the need for 0.3 mm CSP pitch within 7 years, so significant development efforts will be required to provide substrates that can support such fine pitches.

Reliability Concerns for Missile Applications

The basic reliability concerns for any package construction involve the interfacial adhesion of materials and the diffusion of materials. Table 1 highlights some of the principal characteristics of the materials involved in CSP devices and the mounting substrate, typically an epoxy glass (FR-4) PWB. Mold compound properties can vary greatly depending on the fillers and the particular chemical formulation of the epoxy resin, so the values cited in Table 1 should not be used for specific evaluations. In addition, all these characteristics generally vary with temperature, and can have dramatic temperature coefficients over the typical range of use from -40°C to above $+100^{\circ}\text{C}$. In addition, moisture affects the adhesion and other properties of many packaging materials, particularly, the polymeric materials. For particular materials, any analysis of assembly reliability should assess the properties over temperature, as well as other constitutive model parameters, such as creep. Figure 6 shows the basic structure involved in CSP assemblies.

Missile applications typically require high reliability from the electronics, and should survive long term storage, and field handling and use. These environments can subject the electronics to humidity, temperature cycling, and various mechanical vibrations and shocks. The test data available on CSPs generally consists of single environments (but often with preconditioning to simulate solder attach reflow conditions), as now performed on conventional SMT packages. At the assembly level, most of the reliability testing to date involves daisy-chain wired CSPs (in lieu of functional IC chips) to support evaluation of the solder joints. As an isolated package, the CSP sees far less stress than in the assembly during temperature cycling and any mechanical stress, since once attached to a substrate far greater thermal expansion differences come into play and mechanical effects can be transmitted to the various CSP interfaces within the package (Reference 10). These effects necessitate the testing of CSPs after attachment to the intended substrate type. Even the thickness of the substrate could influence the integrity of the solder joints as well as other structures and interfaces of the CSP. Thermal mismatch causes the greatest strain on the typical CSP assembly.

At the same time that the PWB significantly influences the stresses on the CSP, the small pitches of CSPs require advances in PWB interconnections, particularly for high I/O count devices. To access three rows of connections on a CSP requires that two traces run between adjacent pads on the outer row. At 0.3 mm pitch, the traces width

should not exceed 30 μm and the spacing should not exceed 35 μm . Such trace dimensions still require

Material	Coefficient of Thermal Expansion, ppm/ $^{\circ}\text{C}$	Poisson's Ratio	Elastic Modulus, GPa	Flexural Strength, MPa
Silicon	3	0.28	190	62
Mold Compound	15	0.28	26	70
Solder	25	0.36	41	28 (shear strength)
Polyimide	17	0.30	4	90
FR-4 PWB	15	0.25	18	350
Underfill resin	28	0.30	7	-

Table 1. Some general mechanical properties of CSP materials

significantly more development effort (Reference 4). To support these trace dimensions and provide sufficient via density requires the incorporation of build-up technology microvia PWBs in lieu of plated-through hole technology. Plated-through holes typically require significant board space around the hole, whereas, the microvia approach can exist within the outline of the PWB lands that require interconnection, saving PWB real estate for traces, and allowing higher I/O counts and density. The various microvia implementation methods basically all result in complex structures with many material structures and interfaces. Evaluation of CSPs should also address the reliability of these complex substrates.

To illustrate the primary issue of solder joint reliability in connecting the CSP to the substrate, consider the construction shown in Figure 6. The strain, δ , in the second level interconnect solder balls connecting the CSP to the substrate due to thermal expansion mismatch is

$$\delta = \frac{DNP(\alpha_c \Delta T_c + \alpha_s \Delta T_s)}{h}$$

where,

- DNP = the distance to the neutral position point,
- $\alpha_{c,s}$ = thermal expansion coefficient of chip and substrate,
- $\Delta T_{c,s}$ = change in temperature of the chip and substrate, and
- h = the height of the solder ball.

Using the values from Table 1 for a typical CSP construction shows that strain range can exceed 2%, a level at which further assessment of actual units is required to determine the fatigue life of the solder joints.

The recent increased use of plastic encapsulated microcircuits and discrete semiconductor devices in military systems required the development of criteria that such device package construction should meet to assure success in missile applications. Appendix A provides the description of the criteria implemented on some

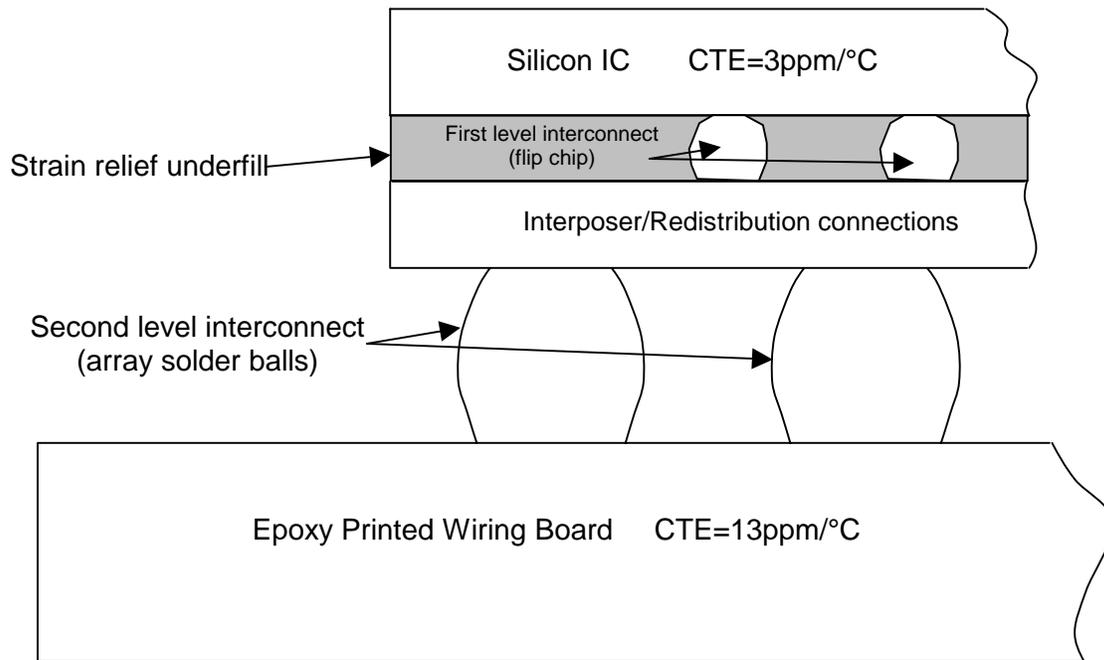


Figure 6. Illustration of packaging challenge to accommodate the strain generated by the CTE mismatch between the IC and substrate.

programs supported by the Aviation and Missile Command. The research that provided the background for these criteria indicated that very little public information exists to support reliability predictions for long-term storage and low duty-cycle operation of the mainstream plastic packages, such as SOICs and PLCCs, in use now. The primary difficulties in reliability prediction involve interfacial adhesion reliability among materials, and manufacturing variation of material properties. In general, detailed characterizations of wear-out mechanisms exist, but as IC device technologies extend to 100 nm feature sizes, basic issues, such as dielectric strength, arise again. The SIA cites the challenges with reliability prediction and accelerated test development in the 1997 Technology Roadmap (Reference 4) and also notes that all new package designs won't have appropriate use in all applications.

Summary

The use of CSPs and related package styles could provide many advantages for missile and related applications that require minimal weight/volume and high electrical performance. Appendix B suggests an outline of a plan to assess how CSPs will perform in missile and other military environments to address the following primary concerns:

Reliability Assessments Required for CSPs

- High-density interconnection substrates (PWBs)
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Acknowledgement

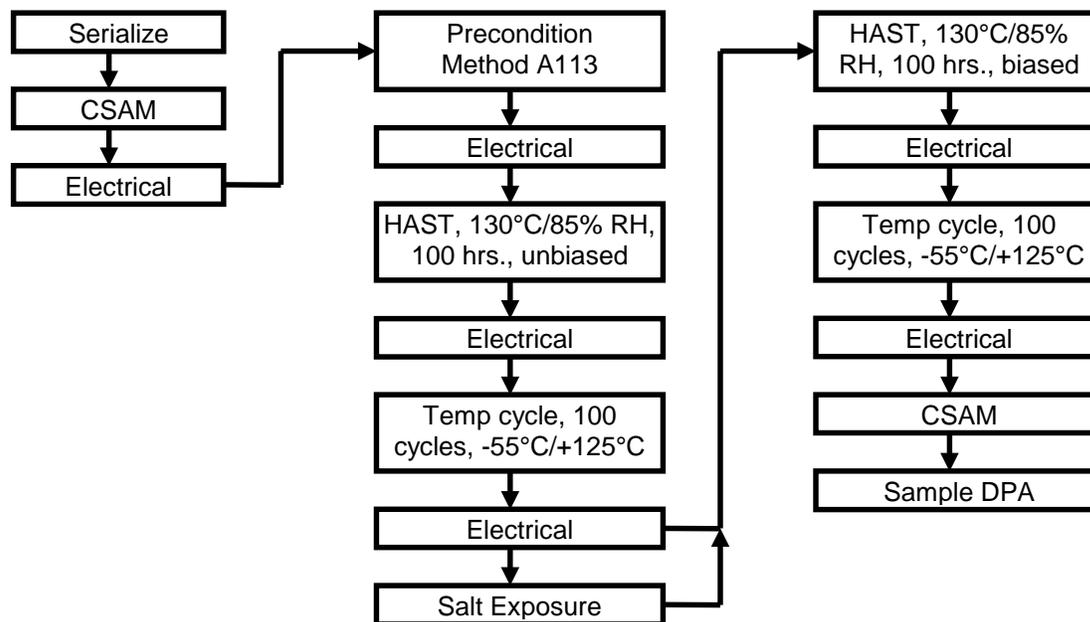
The Air and Missile Defense Program Executive Office funded this effort.

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Appendix A

LONGBOW PEM Qualification Test Sequence



HAST: Highly Accelerated Stress Test, JEDEC-STD 22, Method A110

CSAM: C-mode Scanning Acoustic Microscopy

DPA: Destructive Physical Analysis

Test Philosophy

Insufficient data on PEMs exist to derive a qualification plan based on physics-of-failure and the device construction and materials; however, the above test sequence intends to implement physics-of-failure concepts along with engineering judgment and conservatism to best assess whether particular PEMs can meet typical missile 10 year storage requirements and 20 year storage goals. The initial temperature/humidity exposure is intended to simulate humidity exposure in storage. Temperature/humidity tends to act on all the interfaces, whereas, temperature cycling primarily would stress the interfaces at the die edges from thermal expansion coefficient differences. Humidity first, followed by temperature cycling, will provide more realistic package degradation, by allowing for temperature cycle effects of the generated delaminations and interface weaknesses. The subsequent HAST and TC routines will then allow acceleration of effects that occur after this package degradation. For instance, moisture and ionic contaminant transfer through passivation defects, wire bond shearing due to stress concentrations from delamination voids near the bond pad, etc.

In general, the common degradation mechanisms depend on temperature according to the Arrhenius model, as follows:

$$AF = \frac{K_{r,high}}{K_{r,use}} = e^{\frac{E_a}{k} \left(\frac{1}{T_{use}} - \frac{1}{T_{high}} \right)}$$

Unfortunately, many competing mechanisms exist with different activation energies, E_a , and the activation energy may vary with temperature, and device construction. Worst case mechanisms have activation energies around 0.5 eV, although some exist down to 0.3 eV and up to over 1 eV. A qualification plan should assume a low activation energy, since it requires the longer test time to confirm that such low activation energies do not exist (lower acceleration factor).

Various models have predicted the humidity acceleration to follow the Arrhenius form, $e^{A*(RH_{test}/RH_{use})^n}$, or the power law form, $(RH_{test}/RH_{use})^c$, where A , n , c are model constants, and RH_{test} represents the test relative humidity and RH_{use} represents the use condition relative humidity. Peck and Hallberg summarized several models, and presented data from several studies. Very little data exists for humidity levels below 70% RH, and the humidity acceleration varies with temperature. The various models present widely varying predictions for acceleration factors going from 85% RH to 30% RH. Several studies have utilized two humidities to characterize the model parameters, but this approach assumes a form (such as exponential instead of linear), and so does not reasonably establish any acceleration factor beyond the tested humidity levels. The most optimistic assumption for a qualification plan should be for $c = 1$ in the power-law model based on the available data.

Temperature cycling effects are generally modeled by the Manson-Coffin relationship.

$$\frac{N_{test}}{N_{app}} = \left(\frac{\Delta T_{app}}{\Delta T_{test}} \right)^n$$

The constant, n , requires experimental characterization, but little data presently exists to establish this constant for surface PEM construction. For previously characterized degradation mechanisms, these values range from 1.2 to 2. A qualification plan should assume values towards the pessimistic end when little data exists to justify a value. At $n = 1.35$, a test of 200 cycles from -55°C to $+125^\circ\text{C}$ would equate to 9 years of 20°C diurnal cycling and 1 year of 30°C diurnal cycling.

With very pessimistic assumptions, the test sequences equate to about 8 years of life for the tested environments, yet with optimistic assumptions one could argue that the sequence equates to over 100 years. A qualification plan should provide high confidence that a particular design and construction will meet system requirements, so the plan should lean towards the pessimistic side in its assumptions. Since actual use should provide better performance than these pessimistic assumptions, the test should provide good confidence that the devices will meet the system requirements and goals.

The effects of ionic contamination would remain mostly uncharacterized, and future work will be required to better characterize this risk. Some evaluations of circuit card assembly ionic contaminant residues indicate levels in the $10 \mu\text{g}/\text{in}^2$ region. Since this concentration roughly equals the concentration within the package molding compounds, if these external sources diffused into the package, the lifetime could be reduced by half compared to no external sources (as in the typical HAST condition with deionized water). If the life can be shown to provide a 2X margin with respect to the requirement under "clean" test conditions, then one could have high confidence that even with external ionic contaminant sources the parts would meet system requirements.

With the information available now on PEM failure mechanisms, the proposed plan provides reasonable criteria for assessing PEM life in missile applications in the range of 10 to 20 years of storage and use (with use time on the order of 1 year).

Appendix B

Plan to Evaluate CSPs for Missile Applications

- Task 1. Pursue leveraging of DARPA/Tri-Service Affordable Multi-Missile Manufacturing (AM³), and NAVY MANTECH “Electronics Miniaturization for Missile Applications.”
- Task 2. Develop arrangements to procure particular devices in specific CSP package types. Identify trade-offs in establishing best mix of package types between conventional SMT and CSP/BGA. Some off-the-shelf CSPs exist, but many more would be semi-custom packaging jobs.
- Task 3. Perform testing on assemblies with representative devices and PWB constructions. Test matrix elements to consider:
- Package type/size
 - IC type
 - Substrate technology
 - Flux type
 - Flux cleaning process
 - Conformal coating type
- Task 4. Perform evaluation of test vehicles to assess detailed material, construction, and process properties as necessary to evaluate assembly reliability.

Schedule Element	FY99				FY00			
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
Task 1: Leveraging Arrangements								
Identify areas of cooperation/coordinate efforts								
Task 2: Part selection/Define Test Articles								
Contact CSP manufacturers								
Eval trade-offs and select parts/UUT architecture								
Task 3: Perform Tests								
Develop test matrix/select test facilities								
Procure parts and materials/develop test software								
Assemble units for test								
Perform tests/report results								
Task 4: Perform Follow-on Tests								
Analyze test results								
Define need for test vehicles								
Follow-on tests as needed								