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Manufacturing Technology

DEVELOPMENT OF PLASTIC ENCAPSULATED MICROCIRCUIT COATING PROCESSES FOR MILITARY APPLICATIONS

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Introduction

Former Secretary of Defense Dr. William Perry's memorandum of June 29, 1994, *Specifications & Standards-A New Way of Doing Business*, mandated DOD use of commercial off-the-shelf (COTS) technology wherever possible. This forced weapon system managers and system integrators in the Defense industry to expedite use of plastic encapsulated microcircuits (PEMs), leading to concerns over reliability, field performance, and life-cycle repair costs. COTS integrated circuits (ICs) are usually embedded in an epoxy material (plastic encapsulation) that provides environmental protection to the IC (but not hermetic protection) and mechanical support for the IC's electrical connections to the outside world.

The epoxy material is susceptible to water vapor intrusion, and any impurities within the epoxy material or on the IC can react with the interconnecting metal on the IC using moisture as a catalyst. This often results in corrosion of interconnected wires and bonding pads on the IC, leading to irregular performance and eventual device failure. Powering up PEMs helps to dissipate moisture through component heating, but some Army weapons such as missiles are stored for

long periods without being operated (long-term dormant storage of 10 to 20 years or more). Unfortunately, little data exist to prove that commercially available PEMs will survive this environment. Compounding the problem is the fact that currently used military-grade hermetic parts are rapidly diminishing in availability as manufacturers close their unprofitable military specification markets because of decreased orders from the military (less than one percent of the total semiconductor market). This small market is the primary reason why commercial semiconductor manufacturers are reluctant to meet military requests for increased reliability. To make PEMs a viable replacement for military-grade ceramic-packaged devices, an inexpensive and effective protection scheme must be used to eliminate common failure mechanisms in PEMs. Concurrently, this scheme must add value to commercial applications in a way that encourages semiconductor manufacturers to adopt the protection method. The U.S. Army Aviation and Missile Command's (AMCOM's) Manufacturing Science and Technology Division, working with the Tactical Missile Program Executive Office, has initiated a Manufacturing

Technology (MANTECH) Program to address these issues.

MTO

"Development of Plastic Encapsulated Microcircuit (PEM) Coating Processes for Military Applications" is a DA-approved Manufacturing Technology Objective (MTO) under the Army MANTECH Program. The goal of this effort is to demonstrate and develop a protective coating that can be economically applied, is accepted by the semiconductor industry, and provides the high level of environmental protection required by many military applications. The program leverages previous efforts funded by the Defense Advanced Research Projects Agency (DARPA) and the Air Force to develop a protective coating and processes that effectively seal the surface of ICs while still in the wafer form.

A recently completed Air Force Tech Base Program revealed that Dow Corning's ChipSeal™ can provide essentially hermetic protection to ICs that are exposed to highly accelerated stress testing (HAST). Figure 1 shows test data from that program indicating a high failure rate for standard PEMs, while the ChipSeal™-coated PEMs had a very low

failure rate, approaching that of hermetic controls. A microsection view of the ChipSeal™ coating is shown within the dashed line in Figure 2. The ChipSeal™ process uses a spun-on coating of flowable silicon dioxide (SiO₂) to planarize the wafer surface, followed by a topcoat of silicon carbide (SiC) to seal the wafer. Openings to the IC contact pads are then etched through the SiC and SiO₂. The contact pads are covered with a barrier metal of titanium tungsten (TiW) and then with gold (Au), sealing the etched openings and providing excellent electrical contact to the next level interconnect. All processes are accomplished using standard semiconductor manufacturing equipment.

A ChipSeal™ coating or similar approach offers a low-risk solution to the previously stated challenges for military system production. Benefits from such a protective coating include increased applicability of commercial ICs to harsh military environments, unit cost at or below the price of commercial ICs, and increased flexibility for military use of

new and advanced semiconductor packaging. An economic analysis performed on six representative AMCOM systems shows a potential cost avoidance of more than \$357 million for FYs 03 through 14 from the implementation of wafer-level protective coating technology.

AMCOM entered into a 36-month, competitively awarded, cost-shared, cooperative agreement with Lockheed Martin Missiles and Fire Control, Dallas, TX, on June 30, 1999, to execute the Army MANTECH PEM Coatings Program. The total amount of the agreement is more than \$12 million, of which more than \$7 million is contractor cost share. The vertically integrated Lockheed Martin-led team includes the following:

- Lockheed Martin and Boeing (military system integrators),
- TriQuint and Fairchild (semiconductor manufacturers),
- Dow Corning (material and process provider),
- Chip Supply Inc. (wafer brokering and packaging), and
- Johns Hopkins University (inde-

pendent testing).

Program Plan

The major thrusts of this program are to select the best materials and processes for further development and cost reduction; collect reliability and cost data from the processing and testing of wafers coated with the protective material; demonstrate the improved processes on a semiconductor line; qualify selected components from participating weapon system project offices for implementation on their systems; and develop a business case to encourage semiconductor fabricators to incorporate the process and materials for most or all of their products. Planned activities are summarized below.

Material Evaluation And Selection. A literature search will determine if other materials and processes exist that can provide protective benefits similar to ChipSeal™. The material must provide hermetic-like moisture and corrosion protection, not negatively affect the operation of the IC, and be compatible with various semiconductor epitaxial materials and

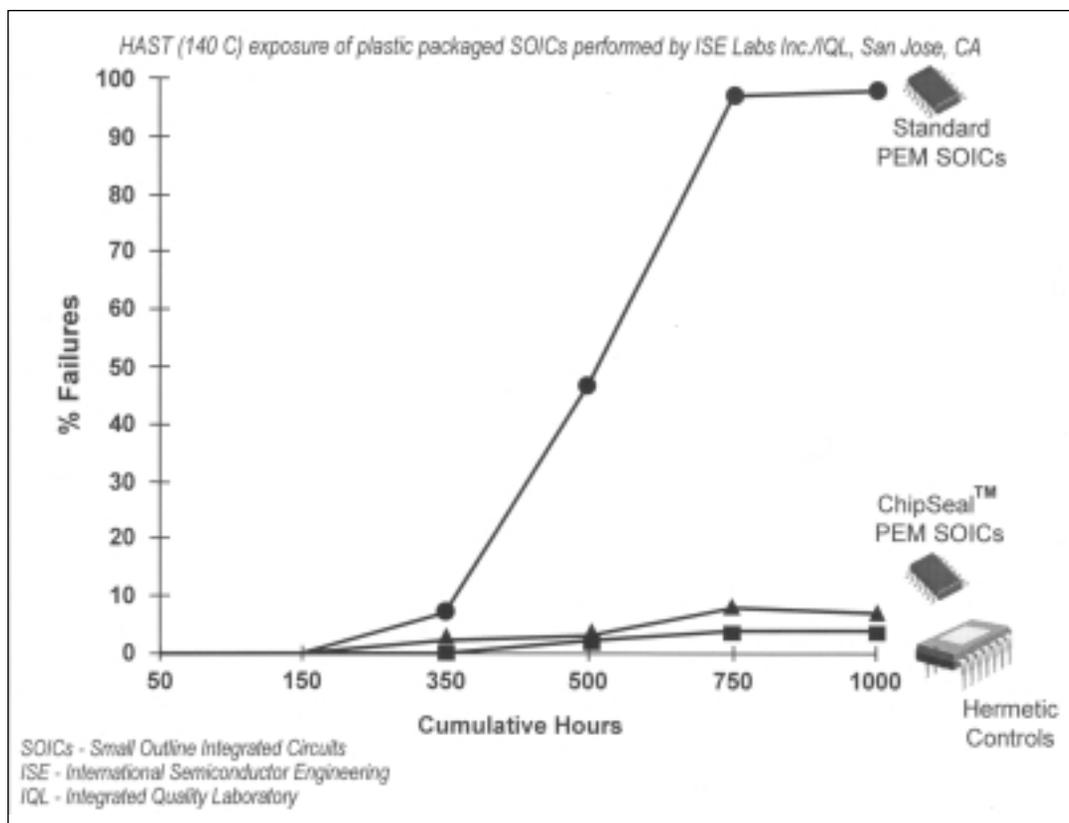


Figure 1.
 ChipSeal™-coated PEM SOIC versus standard PEM SOIC reliability

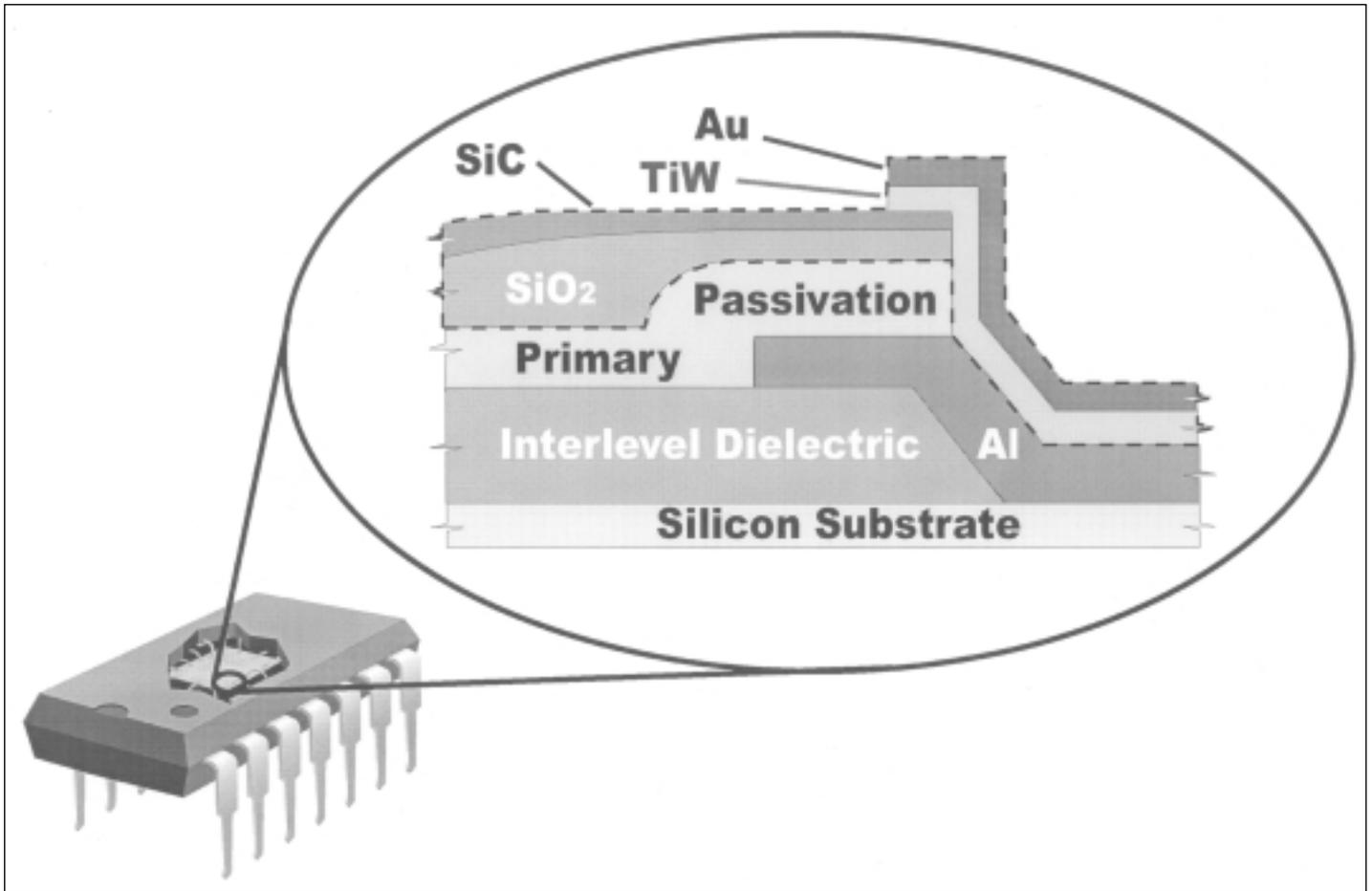


Figure 2.
Microsection view of IC with Dow Corning's ChipSeal™

manufacturing processes. The materials and processes must be inherently very low cost or be able to increase fabrication yields in the downstream packaging process. Both organic and inorganic materials will be studied. Materials and processes that meet the criteria will be selected for use in the remainder of the program.

Silicon And Gallium Arsenide Process Development. Selected coating material(s) and processes will be adapted for the silicon and gallium arsenide fabrication lines at the TriQuint and Fairchild facilities. Methods to lower processing cost and increase processing reliability (i.e., reduce steps, increase repeatability, simplify equipment requirements) will be developed and tested to validate effectiveness of the enhancements. In addition, a reliable under-bump metallization process

for use on flip-chip and chip-scale package applications will be developed. The ChipSeal™ process currently produces an overcoat to the existing passivation layer on an IC. As part of the process development, experiments will be performed to determine if the standard passivation layer (usually silicon nitride) can be eliminated and replaced with the ChipSeal™ coating, reducing protective coating costs by as much as 50 percent.

Component Fabrication. A variety of ICs will be coated and packaged for independent reliability testing. Additional devices, specific to selected Army missiles, will be fabricated with protective coatings for use in hardware qualification tests. The devices will be manufactured at participating semiconductor fabricators' facilities or at a pilot facility, depending on feasibility. Testing will occur at sev-

eral stages of fabrication, and processing information will be gathered to support analysis and modeling efforts.

Data Analysis And Modeling. Test data will be analyzed to determine the coating's impact on the performance and reliability of the ICs. Cost benefits of using the protective coating and its impact on packaging requirements will be studied. Increases in packaging yields will receive special attention because commercial fabricators are constantly struggling to improve yields. Data will also be used to validate the reliability benefits of the protective coating and provide specifics during the business case development. The contractor will also model the process flow as well as update current physics of failure IC models to account for the materials used in the protective coating. Models will be validated

through stress testing and then made available to the electronics design community to aid in future product design.

Independent Component Qualification. Several part types will undergo independent testing by Johns Hopkins University to validate contractor test data. A test plan will be developed by the program team and circulated among national test experts to obtain peer review and consensus.

Military Hardware Subsystem Qualification Testing. Components selected from at least two military systems will be fabricated with the protective coating and packaged as standard PEMs. A test plan similar to the qualification procedures will be developed and executed to demonstrate the reliability of the coated parts in military systems. Preliminary plans are to demonstrate the PEM coating capabilities on a redesigned missile guidance computer for the Army Tactical Missile System and in power supplies used on the Comanche helicopter. Further DOD weapon system demonstrations and implementations are being developed, and more will be solicited during the course of this program.

Business Case And Implementation Plan Development. One very important aspect of this program is to develop the scenarios and reasoning to encourage commercial adoption of this IC protection method. Anticipated benefits of commercial interest are very low implementation and processing costs, little or no impact on the processing line, and yield increases at all fabrication levels. The business case and implementation plan will include significant involvement of the participating commercial semiconductor fabricators, TriQuint and Fairchild. Early adoption of the coating methods will give them an initial advantage over the rest of the industry and serve as a model for further implementations. The implementation plan also calls for development of a strategy to rapidly encourage adoption in the semiconductor industry. A roadmap for weapon system implementation will also be developed.

Government And Industry Workshops

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And Demonstrations. Semiannual government and industry workshops are planned to publicize the ongoing status of the program, solicit feedback, and encourage collaborative efforts toward implementation of the PEM coating techniques. The first workshop is planned for February 2000. An industry demonstration is planned at the end of the program to demonstrate the material(s) and processes in place at a semiconductor fabricator's facility.

Conclusion

The PEM Coating MTO will allow Army weapon system program managers and Defense system integrators to use low-cost PEMs for a much broader range of applications than previously permitted. The use of low-cost PEMs will potentially reduce screening and qualification requirements and reduce life-cycle costs through reduced repair costs and longer life spares. By protecting the IC at the

wafer level, the military can take advantage of smaller, lighter, and higher performance commercial electronic packaging such as flip-chip and chip-scale packages that were previously unsuitable in nonhermetic form. It is inevitable that commercial parts will be increasingly incorporated into DOD systems. The PEM Coating MTO will ensure that COTS chips can be inserted with greater confidence of their reliability in military applications, allowing DOD to keep pace with rapidly advancing commercial technology well into the next millennium.

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